(U.S. patent 6,242,960). Those rejections are respectfully traversed and reconsideration is requested.

Independent claims 1 and 33 are directed to a data transmitter which controls the transition time of a data signal, that is the time that it takes for the data signal to change from one state to the next, a rise time or fall time (page 1, line 7 of the application). As illustrated in Figure 2, an input data signal din has very short transition times from low to high and from high to low. By contrast, the data signal dout has a substantially longer transition time t_r from low to high. This long transition time is obtained by applying the data signal to parallel delay circuits as illustrated, for example, in Figures 1 and 3. The data signal output from each of those delays has a transition time t_{r1} illustrated in Fig. 2. However, by summing the multiple delayed signals at a common output node, it can be seen that the combined transition time of the summed signals d1'-d4' provides the longer transition t_r of signal dout.

Neither of the cited references allows the determination of a transition time of a data signal.

Takada relates to a multiplier circuit that delays a reference signal Fin1 in parallel delay circuits 11 and 13. The outputs of those delay circuits are then added to obtain a multiplied signal having a higher rate than the reference input. Within each delay circuit, a series of delay cells sequentially delays the reference signal under control of a control signal. As illustrated in Fig. 5 the result is that the output of delay circuit 11 and the output of delay circuit 13 are pulses of reduced duration that are displaced relative to each other. By adding the two signals as illustrated in the final line of Fig. 5, a higher rate output is provided. Similarly, in Fig. 6, the last three lines show that the outputs of circuits 11 and 13 are of reduced pulse duration at different times to provide the combined output of a higher rate. Note that in each of Figs. 5 and 6, the time at which each transition occurs is controlled by the control signal; however, the transition times of each pulse, i.e. the rise and fall times, both in the outputs of the delay circuits 11 and 13 and the output of the adder circuit 14, are illustrated to be infinitely short.

The term transition time in the claims must be interpreted in view of the present specification. As illustrated in Figs. 2 and 4, a transition time t_t is the duration of a transition, not the time at which it occurs. Although Takada combines delayed signals, the rise and fall times of the combined signals are non-coincident such that they cannot combine to provide a longer transition time determined by the delays. With the present invention, the combined pulses are nearly coincident so that respective pulses combine to a single pulse having a longer transition as illustrated, for example, in Fig. 2. By contrast, the combined pulses of Takada are distinct and combine to provide plural pulses with no change in transition times.

Each of claims 1 and 33 recites that different delays are applied to a data input and that the delayed data signals are combined in a data output, "a transition time of the data output being determined by difference in delays applied to the data input." Although Takada does combine delayed data signals, those signals are delayed such that, when combined, they provide distinct pulses having the original short transition times. Takada does not address the transition time of an individual signal, that is, the time that it takes for a data signal to change from one state to the next, such as from low to high. Because the combined pulses of Takada are distinct, Takada does not determine the transition time of the data output, that is, a rise time or a fall time (page 1, line 7 of the present application) of the data output.

With respect to claims 18 and 50, prior art transition control systems control the transition time to be a fixed value, regardless of the bit time of the system. With a fixed transition time, a signaling system operating at a lower speed is forced to use a transition time optimized for the highest possible speed of operation, unduly stressing the bandwidth of the transmission medium. In accordance with claims 18 and 50, the transition time of the controlled data signal is proportional to bit time of the bit clock. As already discussed, Takada does not address transition time of a data signal at all, so there can be no suggestion of transition time proportional to bit time.

Nor does Takada teach the dependent claims.